**In the Claims:**

1. (Currently Amended)  A complementary logic circuit, comprising:

a first logic input;

a second logic input;

a first dedicated logic terminal;

a second dedicated logic terminal;

a first logic block comprising:

a p-type transistor network for implementing a predetermined logic

function, said p-type transistor network comprising a plurality of p-type

transistors, and having an outer diffusion connection, a first network gate

connection, and an inner diffusion connection,

said outer diffusion connection of said p-type transistor network being

connected to said first dedicated logic terminal, and said first network gate

connection of said p-type transistor network being connected to said first logic

input; and

a second logic block comprising:

an n-type transistor network implementing logic function complementary

to said predetermined logic function, said n-type transistor network

comprising a plurality of n-type transistors, and having an outer diffusion

connection, a first network gate connection, and an inner diffusion

connection,

said outer diffusion connection of said n-type transistor network being

connected to said second dedicated logic terminal, and said first network gate

connection of said n-type transistor network being connected to said second logic

input;

said inner diffusion connections of said p-type transistor network and of said n-

type transistor network being connected to form a common diffusion logic terminal,

wherein said outer diffusion connection of said p-type transistor network and said outer

diffusion connection of said n-type transistor network are separately configured, such that

said p-type transistor network and said n-type transistor network share a single common diffusion logic terminal.

2. (Original) A complementary logic circuit according to claim 1, wherein said first and second logic inputs are connected to form a first common logic input.

3. (Original) A complementary logic circuit according to claim 1, wherein each of said logic terminals is separately configurable to serve as a logic input.

4. (Original) A complementary logic circuit according to claim 1, wherein each of said logic terminals is separately configurable to serve as a logic output.

5. (Original) A complementary logic circuit according to claim 1, further comprising a third logic input connected to a second network gate connection of said p-type transistor network.

6. (Original) A complementary logic circuit according to claim 1, further comprising a fourth logic input connected to a second network gate connection of said n-type transistor network.

7. (Original) A complementary logic circuit according to claim 5, further comprising a fourth logic input connected to a second network gate connection of said n-type transistor network.

8. (Original) A complementary logic circuit according to claim 7, said third and fourth logic inputs being connected to form a second common logic input.

9-10. (Canceled)

11. (Previously presented) A complementary logic circuit according to claim 1, wherein said p-type transistor network comprises one of a group of networks comprising:

a network of p-type field effect transistors (FET), a network of p-type p-well complementary metal-oxide semiconductor (CMOS) transistors, a network of p-type n-well complementary metal-oxide semiconductor (CMOS) transistors, a network of p-type twin-well complementary metal-oxide semiconductor (CMOS) transistors, a network of p-type silicon on insulator (SOI) transistors, and a network of p-type silicon on sapphire (SOS) transistors.

12. (Previously presented) A complementary logic circuit according to claim 1, wherein said n-type transistor network comprises one of a group of networks comprising: a network of n-type FETs, a network of n-type p-well CMOS transistors, a network of n-type n-well CMOS transistors, a network of n-type twin-well CMOS transistors, a network of n-type SOI transistors, and a network of n-type SOS transistors.

13. (Original) A complementary logic circuit according to claim 2, comprising one of a group of logic circuits comprising: an OR gate, an inverted OR (NOR) gate, an AND gate, a multiplexer gate, an inverter gate, and an exclusive OR (XOR) gate.

14. (Currently Amended) A complementary logic circuit according to claim 12, wherein said logic circuit is operable to implement a ((NOT A) OR B) logic operation upon logic inputs A and B.

15. (Currently Amended) A complementary logic circuit according to claim 12, wherein said logic circuit is operable to implement a ((NOT A) AND B) logic operation upon logic inputs A and B.

16. (Previously presented) A logic circuit, comprising interconnected logic elements, said logic elements comprising:
    a first logic input;
    a second logic input;
    a first dedicated logic terminal;
    a second dedicated logic terminal;

a p-type transistor, having an outer diffusion connection, a gate connection, and an inner diffusion connection; and

an n-type transistor, having an outer diffusion connection, a gate connection, and an inner diffusion connection;

said first logic input being connected to said gate connection of said p-type transistor, said second logic input being connected to said gate connection of said n-type transistor, said first dedicated logic terminal being connected to said outer diffusion connection of said p-type transistor, said second dedicated logic terminal being connected to said outer diffusion connection of said n-type transistor, and said inner diffusion connection of said p-type transistor and said inner diffusion connection of said n-type transistor being connected to form a common diffusion logic terminal, wherein for each of said logic elements each of said logic terminals is separately configurable to serve as a logic output.

17. (Original) A logic circuit according to claim 16, wherein for each of logic elements said first and second logic inputs are connected to form a common logic input.

18. (Original) A logic circuit according to claim 16, wherein for each of logic elements each of said logic terminals is separately configurable to serve as a logic input.

19. (Canceled)

20. (Previously presented) A logic circuit according to claim 16, wherein a type of said p-type transistor comprises one of a group of transistor types comprising: p-type FET transistors, p-type p-well CMOS transistors, p-type n-well CMOS transistors, p-type twin-well CMOS transistors, p-type SOI transistors, and p-type SOS transistors.

21. (Previously presented) A logic circuit according to claim 16, wherein said a type of n-type transistor comprises one of a group of transistor types comprising: n-type FET transistors, n-type p-well CMOS transistors, n-type n-well CMOS transistors, n-type twin-well CMOS transistors, n-type SOI transistors, and n-type SOS transistors.

22. (Currently Amended) A logic circuit according to claim 16<del>17</del>, comprising one of a group of logic circuits comprising: an OR gate, an inverted OR (NOR) gate, an AND gate, a multiplexer gate, an inverter gate, and an exclusive OR (XOR) gate.

23. (Currently Amended) A logic circuit according to claim 16<del>17</del>, wherein said logic circuit is operable to implement a ((NOT A) OR B) logic operation upon logic inputs A and B.

24. (Currently Amended) A logic circuit according to claim 16<del>17</del>, wherein said logic circuit is operable to implement a ((NOT A) AND B) logic operation upon logic inputs A and B.

25. (Original) A logic circuit according to claim 16, further comprising at least one stabilizing buffer element.

26. (Original) A logic circuit according to claim 16, further comprising at least one inverter.

27. (Original) A logic circuit according to claim 16, wherein said logic circuit comprises a C-element.

28. (Original) A logic circuit according to claim 16, wherein said logic circuit comprises a latch.

29. (Original) A logic circuit according to claim 17, comprising one of a group of logic circuits comprising: an SR latch, a D latch, a T latch, and a toggle flip-flop (TFF).

30. (Original) A logic circuit according to claim 16, wherein said logic circuit comprises a bundle data filter controller.

31. (Original) A logic circuit according to claim 16, wherein said logic circuit comprises a one to two decoder.

32. (Original) A logic circuit according to claim 16, comprising one of a group of logic circuits comprising: a carry-lookahead adder (CLA), a ripple adder, a combined ripple-CLA adder, a ripple comparator, a multiplier, and a counter.

33. (Currently Amended) A logic circuit, comprising interconnected logic elements, said logic elements comprising:

a first logic input;

a second logic input;

a first dedicated logic terminal;

a second dedicated logic terminal;

a first logic block comprising:

a p-type transistor network for implementing a predetermined logic function, said p-type transistor network comprising a plurality of p-type transistors, and having an outer diffusion connection, a first network gate connection, and an inner diffusion connection,

said outer diffusion connection of said p-type transistor network being connected to said first dedicated logic terminal, and said first network gate connection of said p-type transistor network being connected to said first logic input; and

a second logic block comprising:

a n-type transistor network implementing logic function complementary to said predetermined logic function, said n-type transistor network comprising a plurality of n-type transistors, and having an outer diffusion connection, a first network gate connection, and an inner diffusion connection,

said outer diffusion connection of said n-type transistor network being connected to said second dedicated logic terminal, and said first network gate connection of said n-type transistor network being connected to said second logic input;

said inner diffusion connections of said p-type transistor network and of said n-type transistor network being connected to form a common diffusion logic terminal, wherein said outer diffusion connection of said p-type transistor network and said outer diffusion connection of said n-type transistor network are separately configured, such that said p-type transistor network and said n-type transistor network share a single common diffusion logic terminal.

34. (Original) A logic circuit according to claim 33, wherein for each of said logic elements said first and second logic inputs are connected to form a first common logic input.

35. (Original) A logic circuit according to claim 33, wherein for each of said logic elements each of said logic terminals is separately configurable to serve as a logic input.

36. (Original) A logic circuit according to claim 33, wherein for each of said logic elements each of said logic terminals is separately configurable to serve as a logic output.

37. (Original) A logic circuit according to claim 33, further comprising a third logic input connected to a second network gate connection of said p-type transistor network.

38. (Original) A logic circuit according to claim 33, further comprising a fourth logic input connected to a second network gate connection of said n-type transistor network.

39. (Original) A complementary logic circuit according to claim 37, further comprising a fourth logic input connected to a second network gate connection of said n-type transistor network.

40. (Original) A complementary logic circuit according to claim 39, said third and fourth logic inputs being connected to form a second common logic input.

41-42. (Canceled)

43. (Previously presented) A logic circuit according to claim 33, wherein said p-type transistor network comprises one of a group of networks comprising: a network of p-type field effect transistors (FET), a network of p-type p-well complementary metal-oxide semiconductor (CMOS) transistors, a network of p-type n-well complementary metal-oxide semiconductor (CMOS) transistors, a network of p-type twin-well complementary metal-oxide semiconductor (CMOS) transistors, a network of p-type silicon on insulator (SOI) transistors, and a network of p-type silicon on sapphire (SOS) transistors.

44. (Previously presented) A logic circuit according to claim 33, wherein said n-type transistor network comprises one of a group of networks comprising: a network of n-type FETs, a network of n-type p-well CMOS transistors, a network of n-type n-well CMOS transistors, a network of n-type twin-well CMOS transistors, a network of n-type SOI transistors, and a network of n-type SOS transistors.

45. (Original) A logic circuit according to claim 33, further comprising at least one buffer element.

46. (Original) A logic circuit according to claim 33, further comprising at least one inverter.

47-54. (Canceled)

55. (Currently Amended) A logic element comprising:
a first logic input;
a second logic input;

a first dedicated logic terminal;

a second dedicated logic terminal;

a p-type transistor, having an outer diffusion connection, a gate connection, and an inner diffusion connection; and

an n-type transistor, having an outer diffusion connection, a gate connection, and an inner diffusion connection;

said first logic input being connected to said gate connection of said p-type transistor, said second logic input being connected to said gate connection of said n-type transistor, said first dedicated logic terminal being connected to said outer diffusion connection of said p-type transistor, said second dedicated logic terminal being connected to said outer 4outer diffusion connection of said n-type transistor, and said inner diffusion connection of said p-type transistor and said inner diffusion connection of said n-type transistor being connected to form a common diffusion logic terminal, said first and second logic inputs being configured as independent inputs, wherein each of said logic terminals is separately configurable to serve as a logic output.

56. (Previously presented) A logic element according to claim 55, wherein each of said logic terminals is separately configurable to serve as a logic input.

57. (Canceled)